UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/677,527	10/02/2000	Chung-Lung Kevin Shum	POU9-2000-0163US1	4322

7590 10/23/2003

Troy J LaMontagne
Cantor Colburn LLP
55 Griffin Road South
Bloomfield, CT 06002

EXAMINER	
ROSS, JOHN M	

ART UNIT	PAPER NUMBER
2188	2

DATE MAILED: 10/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/677,527	SHUM ET AL.	
	Examiner	Art Unit	
	John M Ross	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-26 and 28-35* is/are rejected.

7)☒ Claim(s) *8 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statement(s) received 18 December 2000 has been considered. Please see attached PTO-1449(s).

Drawings

2. The drawings filed on 18 December 2000 have been approved by the Examiner.

Specification

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

Claims 2 and 20 state that the cache coherency protocol of claims 1 and 18 interfaces with the storage controller. However, the cache coherency protocol is self-contained within the bounds of the instruction and data caches of the central processing unit and is merely a statement of policy. It is unclear from the specification how this protocol interfaces with the storage controller because interfacing implies communication between independent entities, whereas the policy statements comprising the protocol do not provide a means for such communication.

Claims 3, 4, 21 and 23 state that the cache coherency protocol of claims 1 and 18 interfaces with existing cache handling requirements. Again, it is unclear from the specification how the policy statements comprising the protocol of claims 1 and 18 interface with the cache handling requirements, which likewise are merely statements of necessary conditions and do not provide a means for the communication implied by interfacing.

For the purposes of examination, claims 2 and 20 will be interpreted to teach that the cache coherency protocol of claims 1 and 18 is combined with the processor system cache coherency protocol employed by the storage controller.

Claims 3, 4, 21 and 23 will be interpreted to teach that the cache coherency protocol of claims 1 and 18 is combined with existing cache handling requirements.

Claim Objections

4. Claims 1-17 and 19-35 are objected to because of the following informalities:

The term "access" (Claim 1, lines 8,10 and 12; claim 13, line 1; claim 19, lines 2,4 and 7; claim 31, line 1) suggests both reading and writing and is therefore inconsistent with the specification, in which only exclusive status is associated with read and write capability (Page 5, lines 6-10).

In order to be consistent with the specification, it is suggested that the term "access" in line 8 of claim 1, line 1 of claim 13, line 2 of claim 19, and line 1 of claim 31 be replaced with "read access" and the term "access" in line 12 of claim 1 and 7 of claim 19 be replaced with

"write access". For clarity, it is suggested that the first instance of the term "access" in line 10 of claim 1 and line 4 of claim 19 be replaced with "read and write access". The claim(s) will be interpreted in light of this suggestion.

The specification defines distinct cache-block statuses among the instruction and data cache (Page 5, lines 15-16 and 20-21). It is unclear in claim 1, lines 9,11 and 13 and claim 19, lines 3,5 and 8 to which cache the status applies. It is suggested that the phrase "in the instruction cache and the operand cache" be inserted after "read only status" in line 9 of claim 1 and line 3 of claim 19. It is also suggested that the phrase "in the operand cache" be inserted after "exclusive status" in lines 11 and 13 of claim 1 and lines 5 and 8 of claim 19. The claim(s) will be interpreted in light of this suggestion.

The phrase "if said cache block has already been accessed by said instruction cache" (Claim 1, line 13; claim 19, lines 8-9) is not consistent with the specification. It is presumed that this phrase is meant to suggest that the cache block has read-only status in the instruction cache. However, merely having been accessed at some time in the past does not require that the block has read-only status as the status may have changed in the intervening time. It is suggested that this phrase be replaced by the phrase "if said cache block has read-only status in the instruction cache". The claim(s) will be interpreted in light of this suggestion.

The phrases "buffering a register of cache locations" and "for fetched unexecuted instructions" (Claim 5, lines 2-3; claim 24, lines 2-3) are unclear and do not reflect the

specification (Page 5, lines 17-24). It is suggested that these phrases be replaced by the phrases "buffering cache block addresses in a register-file" and "corresponding to fetched unexecuted instructions", respectively. The claim(s) will be interpreted in light of this suggestion.

In lines 10-11 of claim 5 and lines 10-11 of claim 24, the phrase "said associated cache block" is improper because an associated cache block has not been previously recited in the claims. It is presumed that the cache block being referred to is that found in line 4 of the claims. It is suggested that the phrase "a cache block's status" (Claim 5, lines 4-5; claim 24, lines 4-5) be replaced by the phrase "an associated cache block's status". The claim(s) will be interpreted in light of this suggestion.

Claims 7 and 26 recite "said request" (Claim 7, lines 2 and 4; claim 26, lines 2 and 4), referring to the request for exclusive status found in lines 5-6 of claims 5 and 24. This may be confused with the requested fetch found in line 12 of claims 5 and 24, respectively. For clarity, it is suggested that this phrase be replaced by the phrase "said request for exclusive status". The claim(s) will be interpreted in light of this suggestion.

The phrase "said probe and" (Claim 8, line 3; claim 27, line 3) " is improper because a probe has not been previously recited in the claims. It is suggested that this phrase be deleted. The claim(s) will be interpreted in light of this suggestion.

The term "I-cache" (Claim 11, line 2; claim 29, line 2) " is improper because an I-cache has not been previously recited in the claims. It is suggested that this term be replaced with "instruction cache". The claim(s) will be interpreted in light of this suggestion.

Claims 17 and 35 recite a "said processor system cache coherency protocol" (Claim 17, lines 1-2; claim 35, lines 1-2), however there is no instance of a processor system cache coherency protocol in the parent claims 16 and 34. However, claims 2 and 20 recite this limitation. It is suggested that claims 16 and 34 be modified to reference claims 2 and 20, respectively. The claim(s) will be interpreted in light of this suggestion.

Claim 20 contains a typographical error. A redundant instance of the word "includes" appears in line 2. It is suggested that this instance be deleted. The claim(s) will be interpreted in light of this suggestion.

All dependent claims are objected to as having the same deficiencies as the claims they depend from.

Appropriate correction of the above noted deficiencies is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-4 and 13-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Anderson (US 3,735,360).

As in claims 1-4 and 13-17, Anderson describes a multi-processor system comprising a pair of parallel and independent caches subjected to a cache coherency protocol and sharing a common main storage (Fig. 1, elements 10, 15 and 16; column 5, lines 18-26), where a cache can have the only copy of a block of data (i.e. exclusive) or one of multiple copies of a block of data (i.e. shared), indicated by a fetch-only bit (Fig. 3, element 62; column 8, lines 10-21) in the cache directory (Fig. 3, element 27; column 5, lines 46-49).

Anderson further describes that when the block of data has exclusive status in a cache, the block may be stored into (i.e. written), but when the block of data is shared it may only be read (Column 8, lines 22-35). This latter state corresponds to a read-only status. Anderson further emphasizes that before a block of data can be stored into, other existing copies must be invalidated and exclusive ownership must be obtained (Column 8, lines 35-39).

Therefore, the protocol described by Anderson may be summarized as:

allowing shared read access by a first cache and second cache to a cache block if the cache block has read-only status in the first cache and the second cache;

allowing read and write access by the first cache and preventing access by the second cache to the cache block if the cache block has exclusive status in the first cache; and

interlocking write access to the cache block by the first cache with exclusive status if the cache block has read-only status in the second cache;

where the first and second caches may be equated with the operand and instruction cache, respectively.

As in claims 2-4 and 16-17, Anderson combines the above cache coherency protocol with existing cache handling requirements and a processor system cache coherency protocol, both employed by a storage control unit, and allowing shared access to cache blocks among a plurality of central processing units (Fig. 1, elements 21,22 and 29-32; column 3, line 64 to column 5, line 8; column 4, line 52 to column 5, line 2; column 5, line 34 to column 6, line 4).

7. Claims 18 and 34-35 are rejected under 35 U.S.C. 102(b) as being anticipated by Gaskins (US 5,930,821).

As in claims 18 and 34-35, Gaskins discloses a system supporting self-modifying code in a processor system (Column 9, lines 19-24) comprising:

a storage controller (Fig. 6, elements 620, 640 and 642); and

a central processing unit (Fig. 6, element 602) including an execution unit (Fig. 6, element 624), an instruction unit (Fig. 6, element 622), and a plurality of caches including a separate instruction cache and operand cache (Fig. 6, elements 605 and 607);

where it is noted that the storage controller function is shown distributed among three elements (Fig. 6, elements 620, 640 and 642) integrated within the central processing unit, yet it may still be interpreted from Fig. 6 of Gaskins that the system further comprises:

the central processing unit coupled to the storage controller;

the execution unit coupled to the instruction unit, the instruction cache and the operand cache;

the instruction unit coupled to the instruction cache and the operand cache; and

the instruction cache coupled to the operand cache.

As in claims 18 and 34-35, Gaskins describes the above system further subjecting the instruction cache and operand cache of the central processing unit to a cache coherency protocol with interlocks on cache block access (Column 3, lines 50-53; Figs. 7 and 8; column 7, lines 60-62; column 8, lines 56-58).

As in claim 34, the processor system of Gaskins includes a plurality of Bus Masters (Fig. 2, elements 110, 112 and 114) that share access to the main memory and level-2 cache (Fig. 2, elements 106 and 108), where it is readily apparent that Bus Masters may include a central processing unit.

As in claim 35, the processor system cache coherency protocol of Gaskins allows the central processing unit to share access to cache blocks with other Bus Masters (Fig. 2, elements 106 and 108; column 2, lines 15-17 and 48-65), where it is readily apparent that Bus Masters may include a central processing unit.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 5-7, 9 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (US 3,735,360) in view of Mahalingaiah (US 6,073,217) and Gaskins (US 5,930,821).

Anderson is relied upon for the teachings relative to claim 3 as above.

As in claims 5-7, 9 and 11-12, Anderson also teaches that when data is required to be stored or updated, an associated cache block's status is evaluated for a desired storage address in a first cache (Fig. 2; column 8, line 55 to column 9, line 3) and a request for exclusive status is transmitted to the storage control unit and a cross-interrogate signal is transmitted to a second cache (Fig. 2; column 9, lines 4-19).

The rationale derived from Anderson in the rejection of claim 3 above is incorporated herein for the teaching of storing in the first cache after exclusive status is obtained via the storage control unit following a response from the cross interrogation.

As in the rejection of claim 3 above, the first and second caches are equated to the operand and instruction cache.

Anderson does not teach the following steps as required by claims 5-7, 9 and 11-12, however, these steps are taught by Mahalingaiah:

buffering cache block addresses in a register-file (Fig. 2, element 48) in an instruction cache (Figs. 1 and 2, element 22) corresponding to fetched unexecuted instructions in an instruction buffer in the instruction unit (Column 3, lines 1-7; column 8, lines 34-37);

discarding and refetching data in the instruction cache if the associated cache block in the instruction cache matches the desired storage address (Column 3, lines 8-12; column 8, lines 41-59);

discarding and refetching data in the instruction buffer and re-buffering cache locations in the register if an instruction stream of an execution unit (Fig. 1, element 28) changes (i.e. if the code is self-modified, see Instant Application, page 6, lines 22-24) (Column 5, lines 13-29 and 54-58; column 8, lines 41-59; column 9, lines 48-60); and

discarding data in the instruction buffer and discarding the cache locations in the register if the execution unit completes execution of fetched instructions (Column 4, lines 13-15; column 8, lines 41-59).

Mahalingaiah teaches that the above steps allow correct execution of self-modifying code (Column 3, lines 12-14; column 5, lines 54-58).

Regarding claims 5-7, 9 and 11-12, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the teachings of Mahalingaiah enumerated above, in the method of Anderson, in order to allow correct execution of self-modifying code as taught by Mahalingaiah.

The combination of Anderson and Mahalingaiah does not teach the following step as required by claims 5-7, 9 and 11-12, however, it is taught by Gaskins:

when instruction fetch is requested, providing the instruction cache read-only status for a requested cache block (Fig. 2, element 205; column 2, lines 18-20; Fig. 8; column 8, lines 58-61).

It is readily apparent from Gaskins that the status for a block in the instruction cache must be read-only because the control unit (i.e. instruction unit) (Fig. 2, element 222) may only fetch instructions and maintains them prior to execution (Column 2, lines 18-27).

Further regarding claims 5-7, 9 and 11-12, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to include the teaching of Gaskins enumerated above, in the method made obvious by the combination of Anderson and Mahalingaiah, because the instruction unit may only fetch instructions.

As in claim 7, Anderson teaches that when exclusive ownership of a cache block is requested, all other copies whether exclusive or read-only are invalidated (Column 8, lines 35-39; column 9, lines 20-32).

As in claims 11-12, Anderson teaches that the cross-interrogation of the cache block address is accomplished via a directory lookup in the storage control unit (Fig. 1, elements 27-28; column 4, lines 20-27 and 56-62; column 5, lines 45-48).

Regarding claim 12, although the combination of Anderson, Mahalingaiah and Gaskin does not teach that the cache directory and register-file comprise six locations, such limitations are merely a matter of design choice and would have been obvious in the method of Anderson, Mahalingaiah and Gaskin. The combination of Anderson, Mahalingaiah and Gaskin teaches both a directory and register file. The limitations in claim 12 of the instant application do not

define a patentably distinct invention since both are directed toward providing storage for indexing cache contents and instruction fetch unit contents. The number of locations is inconsequential for the invention as a whole and presents no new or unexpected result. Therefore, to use six locations would have been an obvious design choice to one of ordinary skill in the art at the time of invention by applicant.

10. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (US 3,735,360) in view of Mahalingaiah (US 6,073,217) and Gaskins (US 5,930,821) as applied to claim 5 above, and further in view of Handy (The Cache Memory Book, Jim Handy, 1998).

Anderson, Mahalingaiah and Gaskins are relied upon for the teachings relative to claim 5 as above.

Anderson further teaches an existing cache handling requirement whereby entries in the cache are replaced according to a replacement algorithm (Column 9, lines 33-39).

Anderson does not teach that the replacement algorithm is a least-recently used replacement algorithm as required by claim 10.

Handy teaches a least recently used cache block replacement algorithm used to determine where to place new blocks of data in a cache (Page 57, paragraph 2).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the least recently used replacement algorithm taught by Handy in the method taught by the combination of Anderson, Mahalingaiah and Gaskin, for the purpose of determining where to place new blocks of data in the cache as taught by Handy.

11. Claims 19-21, 23 and 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaskins (US 5,930,821) as applied to claim 18 above, and in further view of Anderson (US 3,735,360).

Gaskins is relied upon for the teachings relative to claim 18 as above.

Gaskins does not teach the limitations of claims 19-21, and 23 that require the cache coherency protocol to comprise:

the storage controller allowing shared read access by the instruction cache and the operand cache to a cache block if the cache block has read-only status in the instruction and operand caches;

the storage controller allowing read and write access by the operand cache and preventing access by the instruction cache to the cache block if the cache block has exclusive status in the operand cache; and

the storage controller interlocking write access to the cache block by the operand cache with exclusive status if the cache block has read-only status in the instruction cache.

The rationale derived from Anderson in the rejection of claim 1 above is incorporated herein for the teaching of the above cache coherency protocol.

Gaskins also does not teach that shared read access implies that both caches may read a target cache block, that exclusive status dictates sole update access to a target cache block, and that read-only status dictates that a cache block may not be held with exclusive status as required by claims 31-33.

The rationale derived from Anderson in the rejection of claims 13-15 above is incorporated herein for the teaching of the above limitations required by claims 31-33. It is noted that these limitations are a part of the above cache coherency protocol.

Anderson also teaches that the cache coherency protocol (i.e. interlocking mechanism) ensures that a processor accesses the most current data (Column 3, lines 37-44).

Regarding claims 19-21, 23 and 31-33, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the cache coherency protocol enumerated above and taught by Anderson, in the system of Gaskins in order to ensure that a processor accesses the most current data as taught by Anderson.

As in claims 20-21 and 23, Gaskins teaches that the cache coherency protocol is combined with existing cache handling requirements and a processor system cache coherency protocol employed by the storage controller (Column 2, lines 15-17 and 48-65), where it is noted that element 220 in Fig. 2 and element 320 in Fig. 3 both perform the same function as element 620 in Fig. 6.

12. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gaskins (US 5,930,821) in view of Anderson (US 3,735,360) as applied to claim 21 above, and further in view of Handy (The Cache Memory Book, Jim Handy, 1998).

Gaskins and Anderson are relied upon for the teachings relative to claim 21 as above.

Gaskin and Anderson do not teach that the existing cache handling requirements utilize a least-recently used replacement algorithm as required by claim 22.

Handy teaches a cache handling requirement using a least recently used cache block replacement algorithm for determining where to place new blocks of data in a cache (Page 57, paragraph 2).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the least recently used replacement algorithm taught by Handy in the system

made obvious by the combination of Gaskins and Anderson, for the purpose of determining where to place new blocks of data in the cache as taught by Handy.

13. Claims 24-26 and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaskins (US 5,930,821) in view of Anderson (US 3,735,360), and further in view of Handy (The Cache Memory Book, Jim Handy, 1998) as applied to claim 22 above, and further in view of Mahalingaiah (US 6,073,217).

Gaskins, Anderson and Handy are relied upon for the teachings relative to claim 22 above.

Gaskins, Anderson and Handy as applied to claim 22 above, do not teach any of the dependent limitations recited in claims 24-26 and 28-30.

The rationale derived from Gaskins in the rejection of claims 5-7, 9 and 11-12 above is incorporated herein for the following teaching required by claims 24-26 and 28-30:

when an instruction fetch is requested, providing the instruction cache read-only status for a requested cache block.

The rationale derived from Anderson in the rejection of claims 5-7, 9 and 11-12 above is incorporated herein for the following teachings required by claims 24-26 and 28-30:

when data is required to be stored or updated, an associated cache block's status is evaluated for a desired storage address in the operand cache and a request for exclusive status is transmitted to the storage controller and a cross-interrogate signal is transmitted to the instruction cache; and

an operand store is allowed once exclusive status is obtained via the storage controller following a response from the cross interrogation.

Anderson also teaches that the cache coherency protocol (i.e. interlocking mechanism) ensures that a processor accesses the most current data (Column 3, lines 37-44).

Regarding claims 24-26 and 28-30, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the cache coherency protocol enumerated above and taught by Anderson, in the system made obvious by the combination of Gaskins, Anderson and Handy as applied to claim 22 above, in order to ensure that a processor accesses the most current data as taught by Anderson.

Gaskins, Anderson and Handy do not teach the following steps as required by claims 24-26 and 28-30, however, these steps are taught by Mahalingaiah:

buffering cache block addresses in a register-file (Fig. 2, element 48) in an instruction cache (Figs. 1 and 2, element 22) corresponding to fetched unexecuted instructions in an instruction buffer in the instruction unit (Column 3, lines 1-7; column 8, lines 34-37);

discarding and refetching data in the instruction cache if the associated cache block in the instruction cache matches the desired storage address (Column 3, lines 8-12; column 8, lines 41-59);

discarding and refetching data in the instruction buffer and re-buffering cache locations in the register if an instruction stream of an execution unit (Fig. 1, element 28) changes (i.e. if the code is self-modified, see Instant Application, page 6, lines 22-24) (Column 5, lines 13-29 and 54-58; column 8, lines 41-59; column 9, lines 48-60); and

discarding data in the instruction buffer and discarding the cache locations in the register if the execution unit completes execution of fetched instructions (Column 4, lines 13-15; column 8, lines 41-59).

Mahalingaiah teaches that the above steps allow correct execution of self-modifying code (Column 3, lines 12-14; column 5, lines 54-58).

Regarding claims 24-26 and 28-30, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the teachings of Mahalingaiah enumerated

above, in the system made obvious by the combination of Gaskins, Anderson and Handy, in order to allow correct execution of self-modifying code as taught by Mahalingaiah.

The rationale derived from Anderson in the rejection of claim 7 above is incorporated herein for the teaching required by claim 26 that when exclusive ownership of a cache block is requested, all other copies whether exclusive or read-only are invalidated.

The rationale derived from Anderson in the rejection of claims 11-12 above is incorporated herein for the teachings required by claims 29-30 that the cross-interrogation of the cache block address is accomplished via a directory lookup in the storage control unit.

Regarding claims 26 and 29-30, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use the cache coherency protocol enumerated above and taught by Anderson, in the system made obvious by the combination of Gaskins, Anderson, Handy and Mahalingaiah as applied to claim 24 above, in order to ensure that a processor accesses the most current data as taught by Anderson.

Regarding claim 30, although the combination of Gaskins, Anderson, Handy and Mahalingaiah does not teach that the cache directory and register-file comprise six locations, such limitations are merely a matter of design choice and would have been obvious in the system of Gaskins, Anderson, Handy and Mahalingaiah. The combination of Gaskins, Anderson, Handy and Mahalingaiah teaches both a directory and register file. The limitations in claim 30 of the

instant application do not define a patentably distinct invention since both are directed toward providing storage for indexing cache contents and instruction fetch unit contents. The number of locations is inconsequential for the invention as a whole and presents no new or unexpected result. Therefore, to use six locations would have been an obvious design choice to one of ordinary skill in the art at the time of invention by applicant.

Allowable Subject Matter

14. Claims 8 and 27 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, following correction of all other outstanding objections.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M Ross whose telephone number is (703) 305-0706. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

JMR

Reginald G. Bragdon

REGINALD G. BRAGDON
PRIMARY EXAMINER